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EXAMINER	
SAID, MANSOUR M	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,426	YEO ET AL.	
	Examiner	Art Unit	
	MANSOUR M SAID	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in respond to the amendment filed on June 13, 04.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Prior Art (hereinafter referred to as APA) in view of Fujii et al. (; hereinafter referred to as Fujii).

As to claim 1, APA teaches liquid crystal display device (an LCD, (figure 1)) and (specification, (page 3, lines 5-9)) having an interconnection line part (straight line part, (figures 2-3, (20)) and specification, page 4, line 1)) for applying a signal from a driving circuit to (data drive IC) (applying signals through gate/data line(s) a liquid crystal display (specification page 3, lines 9-13 and specification page 4, lines 1-2); comprising a substrate (substrates, (figure 1, (11 & 12)) (specification page 3, lines 9-13); and a plurality of interconnection lines (plurality straight lines part, (figures 2-3, (20)) on the substrate (substrates, (figure 1, (11 & 12)), the interconnection lines (straight line part, (figures 2-3, (20)), a center portion (center portion, (figure 2)) of the interconnection line part (straight line part, (figures 2-3, (20)), and an outer

portion (outer circumference, (figure 2)) of the interconnection line part (straight line part, (figures 2-3, (20)) (specification page 3, lines 20-25 and page 4, lines 1-3).

APA does not expressly teach that the interconnection lines are wider at a center portion of the interconnection line part than at an outer portion of the interconnection line part.

However, Fujii fairly teaches that the interconnection lines (inclined linear wiring, (figure 1, (42-1-42-8)) are wider at a center portion of the interconnection line part (center line, (figures 1-5, (44) than at an outer portion (inclined linear wiring, (figures 1-5, (42-8)) of the interconnection line part (figures 1-5); column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Fujii's an LCD device having wider part on the on the middle part of the lines into APA's an LCD device so as to improve the display quality by optimizing the geometry of transparent electrode formed on the liquid crystal display element substrate (column 1, lines 10-12).

As to claim 2, APA teaches wherein each respective interconnection line ((straight line part, (figures 2-3, (20))) includes a first straight-line part ((first straight line part, (figures 2-3, (20)) to which the driving IC (specification page 4, lines 1-2); a second straight-line part (second straight line part, (figures 3, (20')) connected to gate lines or data lines (gate/data line, (figures 2-3, (20)) of an LCD panel (specification page 3, lines 20-22 and page 4, lines 1-2); and a slanted part (slanted part, (figures 2-3, (21)) for connecting the first straight-line (first straight line part, (figures 2-3, (20)) part with the second straight-line part (second straight line part, (figures 3, (20')) (figures 2-3; (specification page 3, lines 20-22 and page 4, lines 1-2).

As to claim 3, APA teaches wherein the respective interconnection lines are thickly formed in only the first (first straight line part, (figures 2-3, (20)) and second straight-line parts (second straight line part, (figures 3, (20')) (as can be seen from figure, the 1st & 2nd straight lines have thickly formed limes) (specification page 3, lines 20-22 and page 4, lines 1-2).

4. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Hayakawa et al. (6,172,732 B1; hereinafter referred to as Hayakawa).

As to claim 4, APA teaches a liquid crystal display device comprising (an LCD, (figure 1)) and (specification, (page 3, lines 5-9)) a plurality of interconnection lines (plurality straight lines part, (figures 2-3, (20)) for applying a signal from a driving circuit to a liquid crystal display panel (figures 1-3, (20)) (specification page 3, lines 11-15; page 3, lines 20-25 and page 4, lines 1-3).

APA does not expressly teach that a plurality of supplementary conductive patterns

However, Hayakawa teaches a plurality of supplementary conductive patterns (oblique straight wiring conductors (figure 1, (45-1 to 45-10)); abstract; and column 6, lines 28-44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hayakawa's an LCD having a conductive wiring into APA's device so as to provide a more reliable display panel.

As to claim 5, Hayakawa teaches wherein the supplementary conductive patterns (oblique straight wiring conductors (figure 1, (45-1 to 45-10)) are of the same materials as gate lines or data lines of the liquid crystal display panel. (figure 1, column 6, lines 28-44 and column 12, lines 10-15).

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Hayakawa as applied to claim 4 above, and further in view of Fujii.

APA and Hayakawa disclose all claimed limitations except that the interconnection lines are wider at a center portion of the interconnection line part than at an outer portion of the interconnection line part.

However, Fujii fairly teaches that the interconnection lines (inclined linear wiring, (figure 1, (42-1-42-8)) are wider at a center portion of the interconnection line part (center line, (figures 1-5, (44) than at an outer portion (inclined linear wiring, (figures 1-5, (42-8)) of the interconnection line part (figures 1-5); column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Fujii's an LCD device having wider part on the on the middle part of the lines into APA's modified device so as to improve the display quality by optimizing the geometry of transparent electrode formed on the liquid crystal display element substrate (column 1, lines 10-12).

6. Claims 7, 13, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Hayakawa, and further in view of Fujii.

As to claim 7, APA teaches liquid crystal display device (an LCD, (figure 1)) and (specification, (page 3, lines 5-9)) having an interconnection line part (straight line part, (figures 2-3, (20)) and specification, page 4, line 1)) for applying a signal from a driving circuit to (data drive IC) (applying signals through gate/data line(s) a liquid crystal display (specification page 3,

lines 9-13 and specification page 4, lines 1-2); comprising a substrate (substrates, (figure 1, (11 & 12)) (specification page 3, lines 9-13); and a plurality of interconnection lines (plurality straight lines part, (figures 2-3, (20)) on the substrate (substrates, (figure 1, (11 & 12)), the interconnection lines (straight line part, (figures 2-3, (20)), a center portion (center portion, (figure 2)) of the interconnection line part (straight line part, (figures 2-3, (20)), and an outer portion (outer circumference, (figure 2)) of the interconnection line part (straight line part, (figures 2-3, (20)) (specification page 3, lines 20-25 and page 4, lines 1-3).

APA does not expressly teach that the interconnection lines are wider at a center portion of the interconnection line part than at an outer portion of the interconnection line part.

However, Fujii fairly teaches that the interconnection lines (inclined linear wiring, (figure 1, (42-1-42-8)) are wider at a center portion of the interconnection line part (center line, (figures 1-5, (44) than at an outer portion (inclined linear wiring, (figures 1-5, (42-8)) of the interconnection line part (figures 1-5); column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Fujii's an LCD device having wider part on the on the middle part of the lines into APA's an LCD device so as to improve the display quality by optimizing the geometry of transparent electrode formed on the liquid crystal display element substrate (column 1, lines 10-12).

APA and Fujii do not expressly disclose insulating film on the substrate including a conductive layer being electrically connected to a voltage line, and the interconnection lines overlapping the conductive layer.

However, Hayakawa teaches insulating film on the substrate including a conductive layer being electrically connected to a voltage line, and the interconnection lines overlapping the conductive layer (oblique straight wiring conductors (figure 1, (45-1 to 45-10)); column 2, lines 3-20; column 6, lines 28-44; abstract; and column 6, lines 9-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hayakawa's an LCD having a conductive wiring into APA's device so as to provide a more reliable display panel.

As to claim 13, APA and Fujii teach all claimed limitations including a triangle shape on the interconnection lines, but omit to have a conductive layer.

However, Hayakawa teaches insulating film on the substrate including a conductive layer (oblique straight wiring conductors (figure 1, (45-1 to 45-10)); column 6, lines 28-44; abstract; column 2, lines 3-7; and column 6, lines 9-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hayakawa's an LCD having a conductive wiring into APA's device so as to provide a more reliable display panel.

As to claim 15, Hayakawa teaches a plurality of supplementary lines (transparent conductive film, (figure 1, 45-1 to 46-10)) between the interconnection lines (oblique straight wiring conductors (figure 1, (45-1 to 45-10)) and electrically connected with respective interconnection lines (column 6, lines 11-19 and column 27-35).

As to claim 16, Hayakawa teaches wherein the plurality of supplementary lines (transparent conductive film, (figure 1, 45-1 to 46-10)) are formed of the same materials as the

interconnection lines (oblique straight wiring conductors (figure 1, (45-1 to 45-10)) (column 6, lines 11-19 and column 27-35).

As to claim 17, Hayakawa teaches wherein the plurality of supplementary lines (transparent conductive film, (figure 1, 45-1 to 46-10)) is formed with the same size as one another (figure 1).

As to claim 18, APA teaches wherein the interconnection lines (figure 3) are data interconnection lines (specification page 4, lines 1-3).

7. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Hayakawa in view of Fujii as applied to claim 7 above, and further in view of Murade (6,569,717 B1).

As to claims 8-9, APA, Hayakawa and Fujii teach the interconnection lines are wider at a center than an outer portion, but omit to include plurality capacitors.

However, Murade teach plurality capacitors (column 19, lines 29-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Murade's device having plurality capacitors APA's modified system device so as to increase or have a greater capacitance on the wider portion so as to provide a more reliable display panel.

8. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Hayakawa in view of Fujii as applied to claim 7 above, and further in view of Ha (6,493,047 B2).

As to claim 10, APA, Hayakawa, and Fujii teach all claimed limitations in claim 10 except that a voltage for preventing static electricity.

However, Ha teach that a voltage for preventing static electricity (column 1, lines 15-20 and column 8, lines 48-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ha's teaching into APA's modified system so that the switches conductively couple the gate and data lines to each other, reducing or preventing harmful electrostatic discharge (column 3, lines 51-54).

As to claim 11, Ha a common voltage is applied to the conductive layer (column 8, lines 49-53).

9. Claims 12, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Hayakawa in view of Fujii as applied to claim 7 above, and further in view of Moon (6,310,666 B1).

As to claim 12, APA, Hayakawa and Fujii disclose all claimed limitations except that a semiconductor layer doped with impurities.

However, Moon teaches a semiconductor layer (figures 4A-4B, (190)) doped with impurities (column 4, lines 25-31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Moon's device having semiconductor APA's modified system so to prevent a static electricity on the etched surface (column 2, lines 65-67).

As to claim 14, Moon teaches wherein the insulating film (figures 4A-4B, (150)) has a double structure of a gate insulating film and an interlayer insulating film (abstract).

As to claim 19, Moon teaches wherein the conductive layer is formed of the same material as a gate line of the liquid crystal display panel (column 4, lines 15-30).

10. Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Hayakawa, and further in view of Fujii.

As to claim 20, APA teaches liquid crystal display device (an LCD, (figure 1)) and (specification, (page 3, lines 5-9)) having an interconnection line part (straight line part, (figures 2-3, (20)) and specification, page 4, line 1)) for applying a signal from a driving circuit to (data drive IC) (applying signals through gate/data line(s) a liquid crystal display (specification page 3, lines 9-13 and specification page 4, lines 1-2); comprising a substrate (substrates, (figure 1, (11 & 12)) (specification page 3, lines 9-13); and a plurality of interconnection lines (plurality straight lines part, (figures 2-3, (20)) on the substrate (substrates, (figure 1, (11 & 12)), the interconnection lines (straight line part, (figures 2-3, (20)), at center portion (center portion, (figure 2)) of the interconnection line part (straight line part, (figures 2-3, (20)), and an outer portion (outer circumference, (figure 2)) of the interconnection line part (straight line part, (figures 2-3, (20)) (specification page 3, lines 20-25 and page 4, lines 1-3).

APA does not expressly teach that the interconnection lines are wider at a center portion of the interconnection line part than at an outer portion of the interconnection line part.

However, Fujii fairly teaches that the interconnection lines (inclined linear wiring, (figure 1, (42-1-42-8)) are wider at a center portion of the interconnection line part (center line, (figures

1-5, (44) than at an outer portion (inclined linear wiring, (figures 1-5, (42-8)) of the interconnection line part (figures 1-5); column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Fujii's an LCD device having wider part on the on the middle part of the lines into APA's an LCD device so as to improve the display quality by optimizing the geometry of transparent electrode formed on the liquid crystal display element substrate (column 1, lines 10-12).

APA and Fujii do not expressly disclose insulating film on the substrate including a conductive layer.

However, Hayakawa teaches insulating film on the substrate including a conductive layer (oblique straight wiring conductors (figure 1, (45-1 to 45-10)); column 6, lines 28-44; abstract; column 2, lines 3-7; and column 6, lines 9-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hayakawa's an LCD having a conductive wiring into APA's device so as to provide a more reliable display panel.

As to claim 24, Hayakawa teaches a plurality of supplementary lines (transparent conductive film, (figure 1, 45-1 to 46-10)) electrically connected with respective interconnection lines (column 6, lines 11-19 and column 27-35).

11. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Hayakawa in view of Fujii as applied to claim 7 above, and further in view of Ha (6,493,047 B2).

As to claim 21, APA, Hayakawa, and Fujii teach all claimed limitations in claim 10 except that a voltage for preventing static electricity.

However, Ha teach that a voltage for preventing static electricity (column 1, lines 15-20 and column 8, lines 48-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ha's teaching into APA's modified system so that the switches conductively couple the gate and data lines to each other, reducing or preventing harmful electrostatic discharge (column 3, lines 51-54).

As to claim 22, Ha a common voltage is applied to the conductive layer (column 8, lines 49-53).

12. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Hayakawa in view of Fujii as applied to claim 7 above, and further in view of Kwasnick et al. (6,465,824 B1; hereinafter referred to as Kwasnick).

Hayakawa and Fujii disclose all claimed limitations in claim 23 except that the conductive layer is formed of the same material as that of a data line.

However, Kwasnick teaches that the conductive layer is formed of the same material as that of a data line (column 6, lines 60-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kwasnick's teaching into APA's modified system so to increase the versatility of the display device.

13. Claims 25, 27, 29, 31 and 334 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon in view of Fujii).

As to claim 25, Moon teaches a liquid crystal display device (LCD, (figure 3)) having a data interconnection line part (data line, (figures 3 & 4A-4D, (180)) for applying a signal from a driving circuit (driving circuit, (figure 3)) to a liquid crystal display panel (LCD, figure 3)) column 4, lines 13-15 and column 32-37); and a cell array part (pixel electrode, (figure 3, (140)) in which a plurality of gate lines (gate lines, (figure 3, (170)) cross a plurality of data lines (data lines, (figure 3, (180)) to define a pixel region (column 5, lines 15-22), and thin film transistors (TFTS) (TFTS, (figure 3, (131)) are formed at the crossing of the gate lines (gate lines, (figure 3, (170)) and data lines (data lines, (figure 3, (180)), comprising forming a first active layer (semiconductor layer, (figures 4A-4D, (192a)) in an island shape in the region (on figures 4A-4B, the first layer fairly form as an island shape region) where the respective TFTs of the cell (TFT, (figure 3, (131)) array part are formed (see figure 3)) and column 4, lines 40-43), and forming a second active layer (semiconductor layer, (figures 4A-4D, (192b)) on the substrate ((figures 4A-4D, (110)) (column 4, lines 43-45); forming a gate insulating film (insulation layer, (figures 4A-4D, (150)) on the entire surface including the first (figures 4A-4D, (192a)) and second active layers (figures 4A-4D, (192b)) (column 4, 24-30); forming a plurality of gate lines (gate lines, (figure 3, (170)) having gate electrodes (gate electrode, (figures 4A-4D, (170a)

extending therefrom on the first active layer (column 4, lines 20-24); forming source (source electrode, (figures 4A-4D, (180a) and drain regions (drain electrode, figures 4A-4D, (180b) the first active layer (figures 4A-4D, (192a)) by impurity ion implantation using the gate electrodes (gate electrode, (figures 3 & 4A-4D, (170a) as a mask layer in the second active layer (figures 4A-4D, (192b)) (column 4, lines 20-32 and column 4, lines 40-54); forming an interlayer insulating film (protection layer, (figures 4A-4D, (155)) on the entire surface of the source (source electrode, (figures 4A-4D, (180a) and drain regions to (drain electrode, figures 4A-4D, (180b) form a contact hole (contact hole, (figures 4A-4D, (137)), column 4, lines 35-45 and column 5, lines 26-32) and forming a plurality of data lines (data lines, (figure 3, (180)) and data interconnection lines (data lines, (figure 3, (180)), the data lines (data lines, (figure 3, (180)) connected to the source (source electrode, (figures 4A-4D, (180a) and drain regions (drain electrode, figures 4A-4D, (180b) (see figure 3) and formed substantially perpendicular to the gate lines (gate lines, (figure 3, (170)) (see figure 3).

Moon does not expressly teach that so that the data interconnection line part has a wider area in a center portion of the data interconnection line part than in an outer portion of the data interconnection line part and a capacitance of the data interconnection lines with the second active layer is gradually increased towards the center portion from the outer portion.

However, Fujii fairly teaches that the data interconnection lines (inclined linear wiring, (figure 1, (42-1-42-8)) are wider at a center portion of the data interconnection line part (center line, (figures 1-5, (44) than at an outer portion (inclined linear wiring, (figures 1-5, (42-8)) of the interconnection line part (figures 1-5); column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54), since the center portion is wider, therefore it obvious that

a capacitance of the data interconnection lines is gradually increased towards the center portion (see figure 1).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Fujii's an LCD device having wider part on the on the middle part of the lines into Moon's an LCD device so as to improve the display quality by optimizing the geometry of transparent electrode formed on the liquid crystal display element substrate (column 1, lines 10-12).

As to claim 27, Moon teaches a liquid crystal display device (LCD, (figure 3)) having a data interconnection line part (data line, (figures 3 & 4A-4D, (180)) for applying a signal from a driving circuit (driving circuit, (figure 3)) to a liquid crystal display panel (LCD, figure 3)) column 4, lines 13-15 and column 32-37); and a cell array part (pixel electrode, (figure 3, (140)) in which a plurality of gate lines (gate lines, (figure 3, (170)) cross a plurality of data lines (data lines, (figure 3, (180)) to define a pixel region (column 5, lines 15-22), and thin film transistors (TFTS) (TFTS, (figure 3, (131)) are formed at the crossing of the gate lines (gate lines, (figure 3, (170)) and data lines (data lines, (figure 3, (180)), comprising forming a plurality of gate lines (gate lines, (figure 3, (170)) having gate electrodes (gate electrode, (figures 4A-4B, (170a)) in the region where the TFTs are formed (figures 3 & 4A-4B and column 4, lines 14-23) and simultaneously forming a gate metal (metal, such as aluminum) (pattern layer (column 4, lines 17-22); forming a gate insulating film (insulation layer, (figures 4A-4D, (150)) on the entire surface including the gate line (gate lines, (figure 3, (170)) and the gate metal pattern layer (metal, such as aluminum) (column 4, lines 24-30); forming a first active layer (semiconductor layer, (figures 4A-4D, (192a)) in an island shape in the region (on figures 4A-4B; and forming a

plurality of data lines (data lines, (figure 3, (180)) and data interconnection lines (data lines, (figure 3, (180)), the data lines (data lines, (figure 3, (180)) connected to the source (source electrode, (figures 4A-4D, (180a) and drain regions (drain electrode, figures 4A-4D, (180b) (see figure 3) and formed substantially perpendicular to the gate lines (gate lines, (figure 3, (170)) (see figure 3), so that source and drain electrodes are formed on both sides of the active layer (see figures 3 and 4A-4B and column 4, lines 20-45).

Moon does not expressly teach that so that the data interconnection line part has a wider area in a center portion of the data interconnection line part than in an outer portion of the data interconnection line part and a capacitance of the data interconnection lines with the second active layer is gradually increased towards the center portion from the outer portion.

However, Fujii fairly teaches that the data interconnection lines (inclined linear wiring, (figure 1, (42-1-42-8)) are wider at a center portion of the data interconnection line part (center line, (figures 1-5, (44) than at an outer portion (inclined linear wiring, (figures 1-5, (42-8)) of the interconnection line part (figures 1-5); column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54), since the center portion is wider, therefore it obvious that a capacitance of the data interconnection lines is gradually increased towards the center portion (see figure 1).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Fujii's an LCD device having wider part on the on the middle part of the lines into Moon's an LCD device so as to improve the display quality by optimizing the geometry of transparent electrode formed on the liquid crystal display element substrate (column 1, lines 10-12).

As to claim 29, Moon teaches a liquid crystal display device (LCD, (figure 3)) having a data interconnection line part (data line, (figures 3 & 4A-4D, (180)) for applying a signal from a driving circuit (driving circuit, (figure 3)) to a liquid crystal display panel (LCD, figure 3)) column 4, lines 13-15 and column 32-37); and a cell array part (pixel electrode, (figure 3, (140)) in which a plurality of gate lines (gate lines, (figure 3, (170)) cross a plurality of data lines (data lines, (figure 3, (180)) to define a pixel region (column 5, lines 15-22), and thin film transistors (TFTS) (TFTS, (figure 3, (131)) are formed at the crossing of the gate lines (gate lines, (figure 3, (170)) and data lines (data lines, (figure 3, (180)), comprising forming a first active layer (semiconductor layer, (figures 4A-4D, (192a)) in an island shape in the region (on figures 4A-4B, the first layer fairly form as an island shape region) where the respective TFTs of the cell (TFT, (figure 3, (131)) array part are formed (see figure 3)) and column 4, lines 40-43), and forming a second active layer (semiconductor layer, (figures 4A-4D, (192b)) on the substrate ((figures 4A-4D, (110)) (column 4, lines 43-45); forming a gate insulating film (insulation layer, (figures 4A-4D, (150)) on the entire surface including the first (figures 4A-4D, (192a)) and second active layers (figures 4A-4D, (192b)) (column 4, 24-30); forming a plurality of gate lines (gate lines, (figure 3, (170)) on gate insulating film (figures 4A-4B, (150)) at the cell array part (pixel electrode, (figure 3, (14)) (column 4, lines 24-30)) and); forming an interlayer insulating film (protection layer, (figures 4A-4D, (155)) on the entire surface of the source (source electrode, (figures 4A-4D, (180a) and drain regions to (drain electrode, figures 4A-4D, (180b) form a contact hole (contact hole, (figures 4A-4D, (137)); and forming a gate metal (metal, such as aluminum) (pattern layer (column 4, lines 17-22) a gate insulating film (insulation layer, (figures 4A-4D, (150)) on the entire surface at the interconnection data lines

(figure 3, (180)) so that a gate electrode (figures 4A-4B) is formed above the active layer ((column 4, lines 20-24); forming an impurity region in the active layer (figures 4A-4D, (192a)) the gate electrodes (gate electrode, (figures 3 & 4A-4D, (170a) as a mask (column 4, lines 20-32 and column 4, lines 40-54), ; forming an interlayer insulating film (protection layer, (figures 4A-4D, (155)) on the entire surface including the gate lines, (figure 3, (170) and gate metal layer so as to form a contact hole (contact hole, (figures 4A-4D, (137)) (column 4, lines 19-53); and forming a plurality of data lines (data lines, (figure 3, (180)) and data interconnection lines (data lines, (figure 3, (180)), the data lines (data lines, (figure 3, (180)) connected to the source (source electrode, (figures 4A-4D, (180a) and drain regions (drain electrode, figures 4A-4D, (180b) (see figure 3) and formed substantially perpendicular to the gate lines (gate lines, (figure 3, (170)) (see figure 3), so that source and drain electrodes are formed on both sides of the active layer (see figures 3 and 4A-4B and column 4, lines 20-45).

Moon does not expressly teach that so that the data interconnection line part has a wider area in a center portion of the data interconnection line part than in an outer portion of the data interconnection line part and a capacitance of the data interconnection lines with the second active layer is gradually increased towards the center portion from the outer portion.

However, Fujii fairly teaches that the data interconnection lines (inclined linear wiring, (figure 1, (42-1-42-8)) are wider at a center portion of the data interconnection line part (center line, (figures 1-5, (44) than at an outer portion (inclined linear wiring, (figures 1-5, (42-8)) of the interconnection line part (figures 1-5); column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54), since the center portion is wider, therefore it obvious that

a capacitance of the data interconnection lines is gradually increased towards the center portion (see figure 1).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Fujii's an LCD device having wider part on the on the middle part of the lines into Moon's an LCD device so as to improve the display quality by optimizing the geometry of transparent electrode formed on the liquid crystal display element substrate (column 1, lines 10-12).

As to claim 31, Moon teaches a liquid crystal display device (LCD, (figure 3)) having a data interconnection line part (data line, (figures 3 & 4A-4D, (180)) for applying a signal from a driving circuit (driving circuit, (figure 3)) to a liquid crystal display panel (LCD, figure 3)) column 4, lines 13-15 and column 32-37); and a cell array part (pixel electrode, (figure 3, (140)) in which a plurality of gate lines (gate lines, (figure 3, (170)) cross a plurality of data lines (data lines, (figure 3, (180)) to define a pixel region (column 5, lines 15-22), and thin film transistors (TFTS) (TFTS, (figure 3, (131)) are formed at the crossing of the gate lines (gate lines, (figure 3, (170)) and data lines (data lines, (figure 3, (180)), comprising forming a first active layer (semiconductor layer, (figures 4A-4D, (192a)) in an island shape in the region (on figures 4A-4B, the first layer fairly form as an island shape region) where the respective TFTs of the cell (TFT, (figure 3, (131)) array part are formed (see figure 3)) and column 4, lines 40-43), and forming a second active layer (semiconductor layer, (figures 4A-4D, (192b)) on the substrate ((figures 4A-4D, (110)) (column 4, lines 43-45); forming a gate insulating film (insulation layer, (figures 4A-4D, (150)) on the entire surface including the first (figures 4A-4D, (192a)) and second active layers (figures 4A-4D, (192b)) (column 4, 24-30); forming a plurality of gate

lines (gate lines, (figure 3, (170)) on gate insulating film (figures 4A-4B, (150)) at the cell array part (pixel electrode, (figure 3, (14)) (column 4, lines 24-30)) and); forming an interlayer insulating film (protection layer, (figures 4A-4D, (155)) on the entire surface of the source (source electrode, (figures 4A-4D, (180a) and drain regions to (drain electrode, figures 4A-4D, (180b) form a contact hole (contact hole, (figures 4A-4D, (137)); and forming a gate metal (metal, such as aluminum) (pattern layer (column 4, lines 17-22) a gate insulating film (insulation layer, (figures 4A-4D, (150)) on the entire surface at the interconnection data lines (figure 3, (180)) so that a gate electrode (figures 4A-4B) is formed above the active layer ((column 4, lines 20-24); forming an impurity region in the active layer (figures 4A-4D, (192a)) the gate electrodes (gate electrode, (figures 3 & 4A-4D, (170a) as a mask (column 4, lines 20-32 and column 4, lines 40-54), ; forming an interlayer insulating film (protection layer, (figures 4A-4D, (155)) on the entire surface including the gate lines, (figure 3, (170) and gate metal layer so as to form a contact hole (contact hole, (figures 4A-4D, (137)) (column 4, lines 19-53); and forming a plurality of data lines (data lines, (figure 3, (180)) and data interconnection lines (data lines, (figure 3, (180)), the data lines (data lines, (figure 3, (180)) connected to the source (source electrode, (figures 4A-4D, (180a) and drain regions (drain electrode, figures 4A-4D, (180b) (see figure 3) and formed substantially perpendicular to the gate lines (gate lines, (figure 3, (170)) (see figure 3), so that source and drain electrodes are formed on both sides of the active layer (see figures 3 and 4A-4B and column 4, lines 20-45).

Moon does not expressly teach that so that the data interconnection line part has a wider area in a center portion of the data interconnection line part than in an outer portion of the data

interconnection line part and a capacitance of the data interconnection lines with the second active layer is gradually increased towards the center portion from the outer portion.

However, Fujii fairly teaches that the data interconnection lines (inclined linear wiring, (figure 1, (42-1-42-8)) are wider at a center portion of the data interconnection line part (center line, (figures 1-5, (44) than at an outer portion (inclined linear wiring, (figures 1-5, (42-8)) of the interconnection line part (figures 1-5); column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54), since the center portion is wider, therefore it obvious that a capacitance of the data interconnection lines is gradually increased towards the center portion (see figure 1).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Fujii's an LCD device having wider part on the on the middle part of the lines into Moon's an LCD device so as to improve the display quality by optimizing the geometry of transparent electrode formed on the liquid crystal display element substrate (column 1, lines 10-12).

As to claim 33, Moon teaches a liquid crystal display device (LCD, (figure 3)) having a data interconnection line part (data line, (figures 3 & 4A-4D, (180)) for applying a signal from a driving circuit (driving circuit, (figure 3)) to a liquid crystal display panel (LCD, figure 3)) column 4, lines 13-15 and column 32-37); and a cell array part (pixel electrode, (figure 3, (140)) in which a plurality of gate lines (gate lines, (figure 3, (170)) cross a plurality of data lines (data lines, (figure 3, (180)) to define a pixel region (column 5, lines 15-22), and thin film transistors (TFTS) (TFTS, (figure 3, (131)) are formed at the crossing of the gate lines (gate lines, (figure 3, (170)) and data lines (data lines, (figure 3, (180)), comprising forming a first active layer

(semiconductor layer, (figures 4A-4D, (192a)) in an island shape in the region (on figures 4A-4B, the first layer fairly form as an island shape region) where the respective TFTs of the cell (TFT, (figure 3, (131)) array part are formed (see figure 3)) and column 4, lines 40-43), and forming a second active layer (semiconductor layer, (figures 4A-4D, (192b)) on the substrate ((figures 4A-4D, (110)) (column 4, lines 43-45); forming a gate insulating film (insulation layer, (figures 4A-4D, (150)) on the entire surface including the first (figures 4A-4D, (192a)) and second active layers (figures 4A-4D, (192b)) (column 4, 24-30); forming a plurality of gate lines (gate lines, (figure 3, (170)) having gate electrodes (gate electrode, (figures 4A-4D, (170a) extending therefrom on the first active layer (column 4, lines 20-24); a plurality of data lines (data lines, (figure 3, (180)) and data interconnection lines (data lines, (figure 3, (180)), the data lines (data lines, (figure 3, (180)) connected to the source (source electrode, (figures 4A-4D, (180a) and drain regions (drain electrode, figures 4A-4D, (180b) (see figure 3) and formed substantially perpendicular to the gate lines (gate lines, (figure 3, (170)) (see figure 3), and simultaneously forming a data metal (metal such as chromium) pattern layer (column 4, lines 15-35).

Moon does not expressly teach that so that the data interconnection line part has a wider area in a center portion of the data interconnection line part than in an outer portion of the data interconnection line part and a capacitance of the data interconnection lines with the second active layer is gradually increased towards the center portion from the outer portion.

However, Fujii fairly teaches that the data interconnection lines (inclined linear wiring, (figure 1, (42-1-42-8)) are wider at a center portion of the data interconnection line part (center line, (figures 1-5, (44) than at an outer portion (inclined linear wiring, (figures 1-5, (42-8)) of the

interconnection line part (figures 1-5); column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54), since the center portion is wider, therefore it obvious that a capacitance of the data interconnection lines is gradually increased towards the center portion (see figure 1).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate Fujii's an LCD device having wider part on the on the middle part of the lines into Moon's an LCD device so as to improve the display quality by optimizing the geometry of transparent electrode formed on the liquid crystal display element substrate (column 1, lines 10-12).

14. Claims 26, 28, 30, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon in view of Fujii as applied to claim 25 above, and further in view of Kwasnick et al. (6,465,824 B1; hereinafter referred to as Kwasnick).

As to claims 26, 28, 30, 32 and 34, Moon and Fujii disclose all claimed limitations except that the supplementary lines is formed of the same material as that of a data line, so as to be electrically connected to the respective data interconnection lines.

However, Kwasnick teaches that the supplementary lines (conductive layer) are formed of the same material as that of a data line, so as to be electrically connected to the respective data interconnection lines (column 6, lines 60-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kwasnick's teaching into Moon's modified system so to increase the versatility of the display device.

Response to Arguments

15. Applicant's arguments filed on June 13, 2004 have been fully considered but they are not persuasive. On page 10, Applicant argued that "none of cited references, single or in combination, teaches or suggests a plurality of interconnection lines on the substrate, the interconnection lines are wider at a center portion of the interconnection line part than the outer portion of the interconnection line part".

However, Examiner respectfully disagrees for the following reason; APA fairly discloses the claimed limitation, such as a plurality of interconnection lines on the substrate (figures 1-3, specification page 3, lines 20-25 and page 4, lines 1-3). APA does not expressly disclose that the interconnection lines are wider at a center portion of the interconnection line part than the outer portion of the interconnection line part".

Fujii's feature fairly shows that the interconnection lines are wider at a center portion of the interconnection line part than the outer portion of the interconnection line part (figures 1-5; column 6, lines 59-67; column 7, lines 15-22 and column 8, lines 45-54).

On pages 11-12, Applicant argued that "none of the cited references, singly or in combination, teaches or suggests at least, a conductive layer being wider at a center portion of the interconnection line part than at an outer portion of the interconnection line part and the conductive layer being electrically connected to a voltage.

APA does not expressly disclose that the interconnection lines are wider at a center portion of the interconnection line part than the outer portion of the interconnection line part".

Fujii's feature fairly shows that the interconnection lines are wider at a center portion of the interconnection line part than the outer portion of the interconnection line part (figures 1-5;

column 6, lines 59-67; column 7, lines 15-22 and column 8, lines 45-54), since the center portion is wider, therefore, it is obvious that a capacitance of the data interconnection lines is gradually increased towards the center portion (see figure 1).

APA and Fujii omit that a conductive layer being electrically connected to a voltage line, and the interconnection lines overlapping the conductive layer.

However, Hayakawa fairly teaches insulating film on the substrate including a conductive layer being electrically connected to a voltage line, and the interconnection lines overlapping the conductive layer (oblique straight wiring conductors (figure 1, (45-1 to 45-10)); column 2, lines 3-20; column 6, lines 28-44; abstract; and column 6, lines 9-19).

On page 13, Applicant argued that none of cited references disclosed, such as, data interconnection lines are wider at a center portion .

However, Fujii fairly teaches data interconnection lines are wider at a center portion (figures 1-5 and column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54).

On page 13, Applicant argued that "none of cited references disclosed that "forming a plurality of gate lines on the gate insulating film at the cell array part and forming a gate metal pattern layer on the gate insulating film at the data interconnection.

However, Moon fairly teaches forming a plurality of gate lines (gate lines, (figure 3, (170)) on gate insulating film (figures 4A-4B, (150)) at the cell array part (pixel electrode, (figure 3, (14)) (column 4, lines 24-30)) and); forming an interlayer insulating film (protection layer, (figures 4A-4D, (155)) on the entire surface of the source (source electrode, (figures 4A-4D, (180a) and drain regions to (drain electrode, figures 4A-4D, (180b) form a contact hole

(contact hole, (figures 4A-4D, (137)); and forming a gate metal (metal, such as aluminum) (pattern layer (column 4, lines 17-22) a gate insulating film (insulation layer, (figures 4A-4D, (150)) on the entire surface at the interconnection data lines (figure 3, (180).

On page 13, Applicant argued that none of the references disclose "forming a plurality of data lines substantially perpendicular to the gate lines to connect source and drain electrode to the impurity region through the contact hole, and simultaneously forming a data metal pattern layer to overlap the gate interconnection line part than at an out portion of the gate interconnection line part.

Moon fairly teaches the claimed limitation such as, forming an interlayer insulating film (protection layer, (figures 4A-4D, (155)) on the entire surface including the gate lines, (figure 3, (170) and gate metal layer so as to form a contact hole (contact hole, (figures 4A-4D, (137)) (column 4, lines 19-53); and forming a plurality of data lines (data lines, (figure 3, (180)) and data interconnection lines (data lines, (figure 3, (180)), the data lines (data lines, (figure 3, (180)) connected to the source (source electrode, (figures 4A-4D, (180a) and drain regions (drain electrode, figures 4A-4D, (180b) (see figure 3) and formed substantially perpendicular to the gate lines (gate lines, (figure 3, (170)) (see figure 3), so that source and drain electrodes are formed on both sides of the active layer (see figures 3 and 4A-4B and column 4, lines 20-45).

However, Fujii fairly teaches data interconnection lines are wider at a center portion (figures 1-5 and column 6, lines 59-67; column 7, lines 15-22; column 7, lines 35-47 and column 8, lines 45-54).

The combination of all cited references fairly disclose the claimed limitation, and therefore, all references should be taken in combination and not individually.

The Applicant cannot show one-obviousness by attacking references individually where, as here the rejections are based on combination of references. In re Keller, USPQ 871 (CCPA 1981).

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS OFFICE ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Mansour M. Said** whose telephone number is **(703) 306-5411**.

The examiner can normally be reached on Monday through Thursday from 8:30 a.m. to 6:00 p.m. The examiner can also be reached on alternate Friday from 8:30 a.m. to 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Shalwala Bipin**, can be reached at **(703) 305-4938**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist)

17. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer service Office whose telephone number is (703) 306-0377.

July 26, 2004

Mansour M. Said

Amare Mengistu
Primary Examiner